# Accelerated Development of Hardware and Software for SOC Design via Co-design and Co-Verification

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***Abstract*— This paper employed Co-design and Co-verification for SOC Design in the transactional level modeling of FPGA. In this investigates, the main advantages of the system provide a centralized method development platform to manage the transaction in TLM. This platform allows designers to use tools such as FPGA, Matlab and Real-View SOC Designers to perform simulation of the system. In final, a powerful method be proposed that speed up the ESL design time and the result is more precise. We suggest that a new design flow which includes models implemented in different abstraction level to be considered together at the same time to make the design process easier.**

***Keywords*— Co-design, Co-Verification, electronic system level, System-on-chip, Transactional Level Modeling**

## 1. INTRODUCTION

The complexity of hardware development becomes extremely high due to the rapid progress of VLSI design tools and the demanding of highly complex systems. New design flows are needed for designers to keep up with the new trend, since it's difficult to carry out huge designs with traditional skills. In recent years, electronic system level (ESL) design has become one of the hottest topics. ESL describes a System-on-chip (SOC) design in the more abstract way and this makes faster system simulation while providing virtual prototypes for hardware and software in co-design and co-verification. It is becoming a fundamental part of overall design flow. Furthermore, incremental design process can be applied to cover different design levels in the same design phase, rather than just in the architecture level and algorithm level.

There are many issues focusing on ESL development. In this paper, we focus on the communication problems in the so-called Transactional Level Modeling (TLM) area. In the past, designers need to take care of both computation units and communication units at the same time. Here, we develop some useful development and interface tools so that the communication problems among computation models are reduced. We provide a centralized system development platform to manage the transaction in TLM. This platform allows designers to use tools such as FPGA, Matlab and Real-View SOC Designers to perform simulation of the system if some models are available in other tools only. Furthermore, one can use multiple computers, each running certain number of models, to work together across internet for remote co-simulation. Hence, engineers could focus on their own modules to make the implementation easier, faster, and more reliable. Finally, we suggest that a new design flow which includes models implemented in different abstraction level to be considered together at the same time to make the design process easier.

## 2. RELATED LITERATURES

The rapid progress of VLSI design and the circuit is more and more complex; we must improve the traditional design techniques for more complex VLSI design. The enhanced technique focuses on accreting the design time that include specification formulation, circuit design, integration and debugging. These steps must spend much time and resources. In figure 1, we compared the traditions and non-traditions in circuit design flow.[1]

In the traditions techniques, it has not provide FPGA test version and DEMO simulation board to software researchers until the hardware design approached to accomplish step. In general condition, no one can guarantee the flow is swimming. For this reason, this paper proposed to advance of the software design time and enhance the precise and efficiency in hardware design. The innovative method is that the start time is the same in design and verification of the hardware/software. The experiment result will indicate to cut down the development time of circuit design, save the design cost and increase the efficiency of entirely system design.[2]

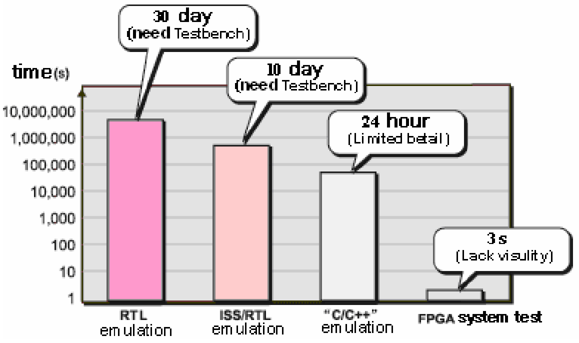


Fig. 1 The circuit design comparison between traditions and non- traditions

According to present design approaches, we employed testbench to Emulate Software for verification hardware circuits. In this paper, we proposed innovative two technologies: 1.Set the EDA co-verification tools to assist hardware simulator operating.2. Employed software debugger tools to input and monitor these program data such as testbench/embedded code. The followings are the advantages via above-mentions technology:[3]

1. To test at good method, the embedded code will be used and act as a testbench.
2. To reduce an ASIC or risk in the test board is error condition.
3. To solve the gray area problems in specification before tape-out

In this study, the main purpose of the innovative approach is that shorten time of system integration. In general SOC design at system software and hardware integration steps is influence circuit physical design, and it is implementing after software verification or application program development based on test-platform. The finished products start production must go through many times correction and integration finished.[4] If the above process has design errors, the test time would be delay. This paper proposed innovative approach that it to curtail system integration time and finished products start production early. The design concept is strong at get the design error part early and will not occurrence idle state.[5][6]

## 3. INTERACTIVE VERIFICATION SYSTEM

The primary key is simulation in fast verification system based on ELS. To utilize model to simulate system functions is fast than RTL, but the time precision is lower. Figure 2 show Speed Comparison of Different ESL/EDA approaches .According to the Chris Lennard and Davorin Mista researches, we join FPGA to electron system layer design tools in system simulation. In fig, 2 right up side, the FPGA based will speed up the design cycle better than above-mentions concept in still more times and the precise ratio is the same.[7]

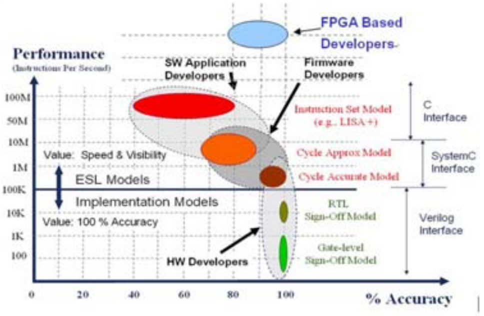


Fig. 2 Speed comparison of different ESL/EDA approaches

In this investigation, we employed software simulator to replace processor of hardware circuits design flow, or to substitute for lung computing and most complex unit completely. The result will be speed up the time of product in development and verification steps.

To review the semiconductor history, when all software/hardware design approaches not enough to the increase complex in design process, the optimal solution is improvement of “Abstraction Level”, than translate it to machine code or electron circuits via EDA tools. In the design of digital circuit field, the first engineer plotted circuits layout at Mylar Film and defined Polygon. ◦ In order to precede more complex circuit design for reaching the high performance, the “Abstraction Level” must be advancement via “Transistor Level”. After accelerated circuits design and verification, we employed synthesizer to translate into Physical Layout and finish the implementation. Move to the scale is more and more larger, the “Abstraction Level” continue to progress toward “Transistor Level “ and “Gate Level” and up to the “Register Transfer Level” (RTL).

From the 1990, the RTL is the primary electron design layer and it succeeds in increasing the gate count to a great many amount. Due to the gate count amount is too larger to hard design for high-speed circuits design via RTL. According to exist researches, we must expand mass computing time and resources for circuits simulation and verification. The lacks of above-monitions are the increase of failure design and influence on the product time schedule.

## 4. EMPLOYED VERILITE TO IMPROVE SOC DESIGN AND VERIFICATION

In this study, we employed ESL to solve the above-mentions problems. Due to the SOC design must consider more tasks such as software/hardware integration simulation and verification, system efficiency analysis, power consumption analysis; therefore the ESL is more important in facing these challenges.

Figure 3 indicated the history of different abstraction layer for complex circuits design with facile and fast.

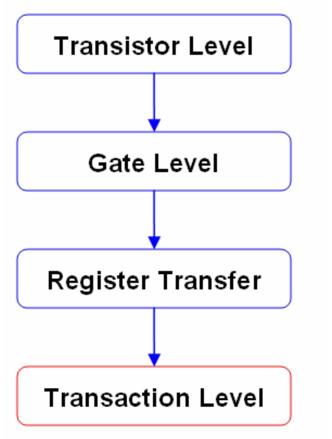


Fig. 3 History of different abstraction layers

We employed VeriLite USB to improve SoC in design verification method with PC-Based FPGA via SMIMS Ltd. The most important ideal is to add Co-design and Co-verification in software/hardware real-time design. The interactive design techniques can cut down the time schedule in a complex SOC system design and verification, fast test and verify the correctness of system circuits, and deliver multimedia information. The method promoted the level of confidence system process and validity in system information.

The VeriLite USB based on design reuse is to reuse previous achievements and not from the beginning, the followings are two ways in the description of design reuse:

1. IP based design：Employed existent IP and add the glue logic to finish design tasks.
2. Platform based design：Employed previous framework of the resemble project to integrate software/hardware for design tasks.

The two methods are design reuse, the first belong to block level reuse, and the second method is system architecture reuse. IP integration is the primary problem in interface module via IP reuse. Interface module defines the IP I/O port signal including data, address, and control data transaction scheme in timing diagram. The advantages of employed platform based design are architecture reuse, some related simulation/ verification model such as bus functional model (BFM) and prototyping system can be reused. The other side, the VeriLite platform regulated operating system for reducing the system development complicated but will influence processor core control and other IP deliver data. The VeriLite platform must establish standard such as OCB、RTOS to proceed soc design, the result of lower complex and fast simulation/ verification tasks.

Figure 4 indicated that the VeriLite USB development board includes FPGA hardware part and another FPGA board connects the host-PC via USB for software running. The Host-PC provided various software and SDK for user send and received the test data and information between Host-PC and FPGA board at the input of top module. This method provided real-time software/hardware Co-design and Co-verification for SOC design via the VeriLite platform.

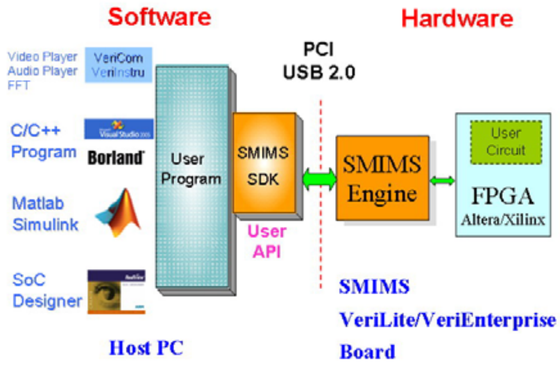


Fig. 4 VeriLite USB development board block diagram.

The system key point is that we employed SMIMS Engine for processing the software/hardware Co-design and Co-verification task at VeriLite USB development board. When VeriLite is operating at application mode, the user FPGA connected the USB device. User designed circuit for processing "user application program" via USB delivery and received. The data transmissions used "FIFO" interface and it consist of signals group including write, read, data input, and data output. Figure 5 show the VeriLite USB development board is operating at application mode.

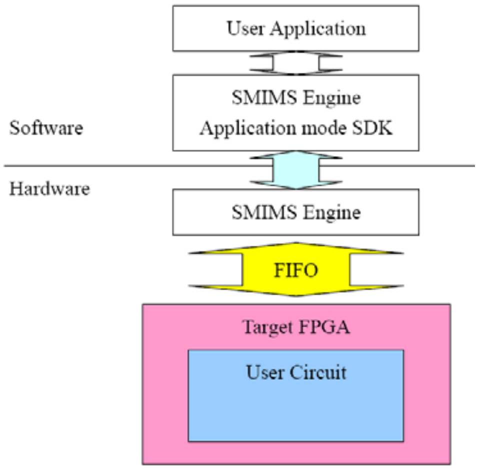


Fig. 5 VeriLite USB development board is operating at application mode.

## 5. ARM BASED SOC DESIGN EXAMPLE VIA VERILITE USB DEVELOPMENT BOARD

The VeriLite® USB provided Altera Cyclone FPGA—EP1C6Q240 for user. The figure show the ARM based SoC design example used VeriLite USB development board

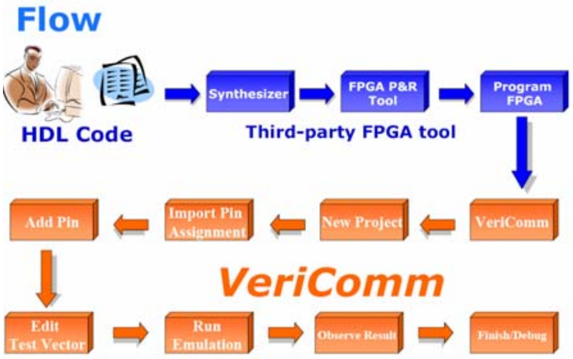
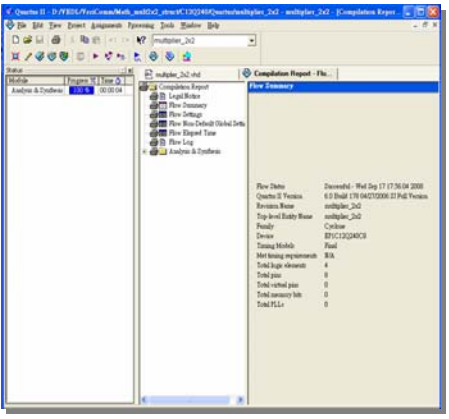


Fig. 6 ARM based SoC design example via VeriLite USB development board.

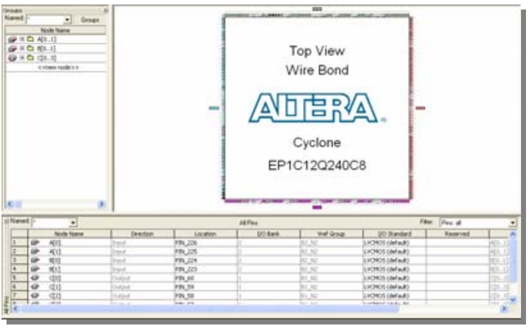
At first, the user employed QuartusII for design of hardware description language. (Two type in VHDL and Verilog) The next we utilized Analysis & Synthesis to check the logical complete and consistence of project and find the boundary connection and syntax error in figure 7(a). Figure 7(b) show the EP1C12Q240C8 pin layout.



Analysis & Synthesis 100 % 00:00:04

Flow Status Successful - Wed Sep 17 17:36:04 2008
Quartus II Version 6.0 Build 178 04/27/2006 SJ Full Version
Revision Name multiplier_2x2
Top-level Entity Name multiplier_2x2
Family Cyclone
Device EP1C12Q240C8
Timing Models Final
Met timing requirements N/A
Total logic elements 4
Total pins 8
Total virtual pins 0
Total memory bits 0
Total PLLs 0

(a)



| | Node Name | Direction | Location | I/O Bank | Vref Group | I/O Standard | Reserved |
|---|---|---|---|---|---|---|---|
| 1 | A[0] | Input | PIN_226 | 2 | B2_N2 | LVCMOS (default) | |
| 2 | A[1] | Input | PIN_225 | 2 | B2_N2 | LVCMOS (default) | |
| 3 | B[0] | Input | PIN_224 | 2 | B2_N2 | LVCMOS (default) | |
| 4 | B[1] | Input | PIN_223 | 2 | B2_N2 | LVCMOS (default) | |
| 5 | C[0] | Output | PIN_60 | 1 | B1_N2 | LVCMOS (default) | |
| 6 | C[1] | Output | PIN_59 | 1 | B1_N2 | LVCMOS (default) | |
| 7 | C[2] | Output | PIN_58 | 1 | B1_N2 | LVCMOS (default) | |

(b)

Fig. 7 The example executed process (1)

After circuits synthesize and write into the FPGA, we used VeriComm to precede the Co-design and Co-verification tasks. After a serial steps, we employed VeriIstrument tool for physical simulation in figure 8.

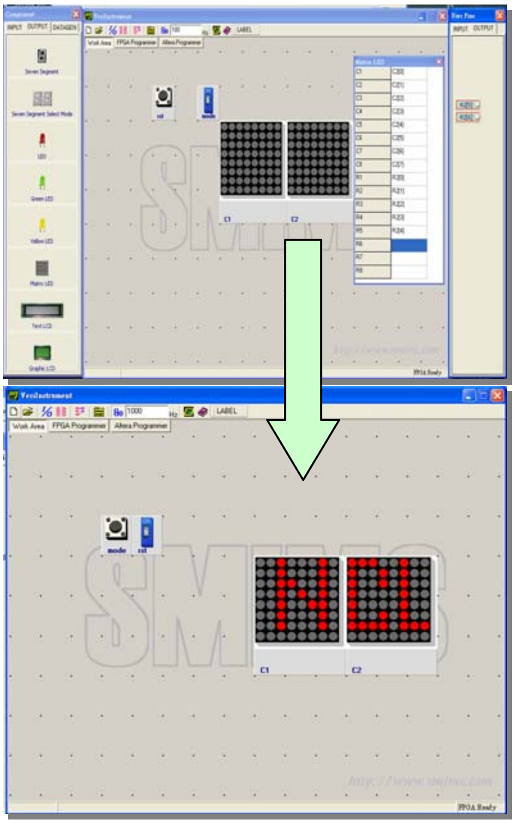


Fig. 8 The example executed process (2)

## 6. Multimedia experiment for co-verification

In the session, we used multimedia input to performance the Co-verification task. Figure 9 indicated the multimedia Co-verification model experiment flow and framework.

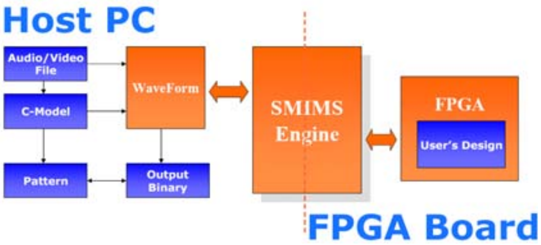
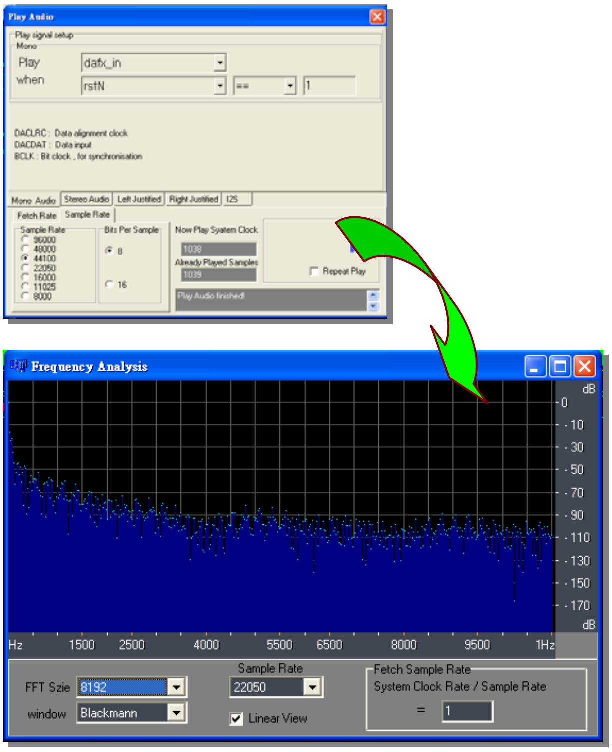


Fig. 9 The multimedia co-verification model.

We suppose to input a sample audio file or real-time recorder at present. The next we setting the audio fetch sample rate. In final the multimedia Co-verification model will produce fast fourier transform (FFT) audio spectrum analysis result in Figure 10.


Play Audio

Play signal setup

Mono

Play: dafx_in

when: rstN == 1

DACLRC : Data alignment clock
DACDAT : Data input
BCLK : Bit clock , for synchronisation

Mono Audio | Stereo Audio | Left Justified | Right Justified | I2S

Fetch Rate | Sample Rate

Sample Rate: ○ 96000 ○ 48000 ● 44100 ○ 22050 ○ 16000 ○ 11025 ○ 8000

Bits Per Sample: ● 8 ○ 16

Now Play System Clock: 1038

Already Played Samples: 1039

□ Repeat Play

Play Audio finished!

Frequency Analysis

FFT Szie: 8192

window: Blackmann

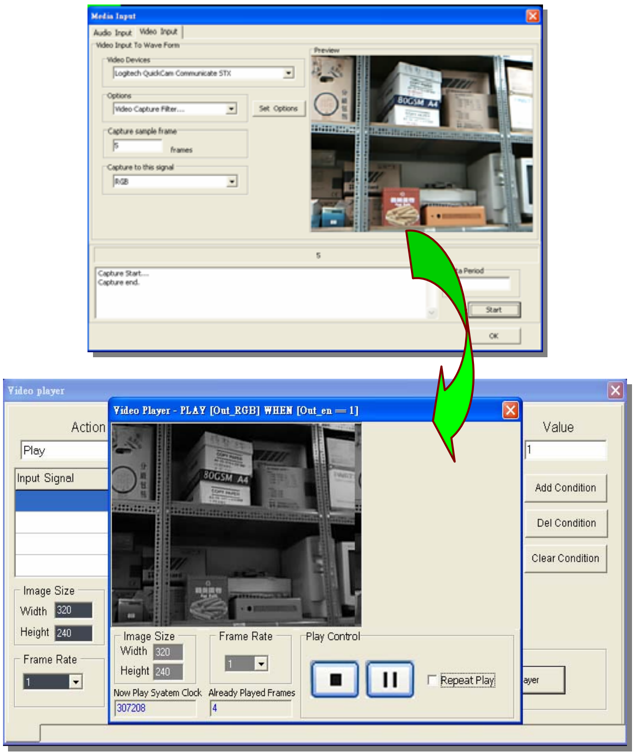
Sample Rate: 22050

☑ Linear View

Fetch Sample Rate: System Clock Rate / Sample Rate = 1

Fig. 10 The sample audio employed FFT to analyze audio spectrum.

Another experiment is video process via real-time video input; figure 11 is the media input sample where it is our wireless sensors network laboratory in national chin-yi university of technology. The video capture sample content is 24 bits format.



Video Devices: Logitech QuickCam Communicate STX

Options: Video Capture Filter...

Capture sample frame: 5 frames

Capture to this signal: RGB

Capture Start....
Capture end.

Action: Play

Value: 1

Input Signal

Image Size Width 320 Height 240

Frame Rate 1

Now Play Syatem Clock 307208

Already Played Frames 4

Fig. 11 The sample video digital signal process.

The “Video Player” provides user for playing the media data by Microsoft DirectShow will reach the effect of real-time surveyed image and video. We can select various decoder for suitable the data format and correctness. Users also employed VeriLite for Co-verification the correctness data and decrease the effort in software development.

This paper proposed an innovative design flow for save more resources reality by VeriLite. The other functions are that VeriLite can combine various tools for synchronism verification and information exchange, these tools such as Matlab, Simulink, Visual c++.Figure 12 show that user employed C and Matlab develop module to interactive deliver data by socket mode. The aim of this paper is common running via develop module in different environment respective. We can easily use co-verification and simulation in the same environment through high abstract layer (such as Matlab module) and lower abstract layer (such as SstemC module) or FPGA hardware module.

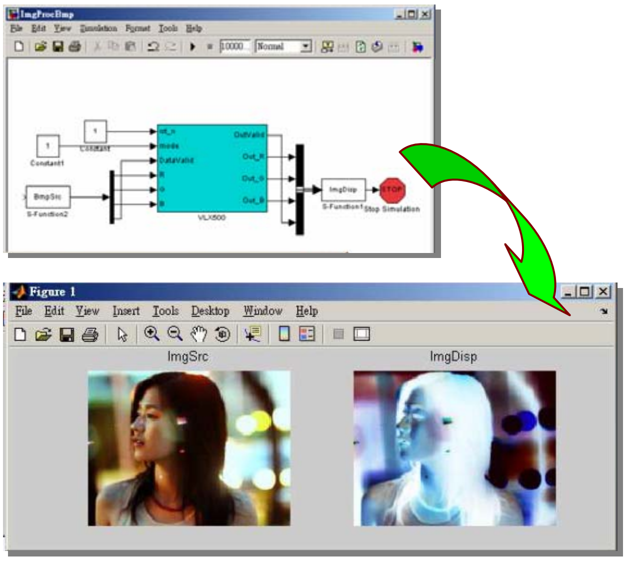


Fig. 12 The simulation using Matlab and Simulink.

## 7. CONCLUSIONS

This study applies the VeriLite and Co-verification tool for integration software and hardware design solution. In this paper, we succeed in employing VeriLit simulate for real-time SOC design and verification in the same time. In this paper, we proposed some tool to reduce artificial lose, fast system integration and debugger. The followings are the advantages of using new design procedure:

1. Controllable
2. Adaptive
3. Observed easily
4. Simple
5. Correctness
6. Speedy

In the simulated experiment, this study performances the Co-verification across different platform by VeriLite. User employed various high-level languages, SOC-designer or Matlab that they may use TLM to co-design in the same platform. This result will carry out Co-design and Co-verification for SOC Design in the transactional level modeling of FPGA.

## ACKNOWLEDGMENT

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