The SFG Modeling Technique for Cascaded Multilevel Inverters with Blanking-Time Effect

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***Abstract*—In this paper, a graphic modeling technique, switching flow-graph (SFG) technique, is applied to derive the large-signal model of cascaded multilevel inverters. By introducing the concept of virtual switch together with its virtual switching function, the modeling work becomes straightforward without complicated mathematic operations. Based on the developed model, the transient and steady state behaviour of cascaded multilevel inverters can easily be analysed at system level. Moreover, the proposed large-signal SFG model can be implemented in MATLAB/SIMULINK environment easily for time domain simulation. Comparison of the simulation results by using the proposed SFG model with that of using PSPICE, one can see that both results are in close agreement. However, the execution time of the proposed SFG model is much shorter than that of using PSPICE, even considering blanking-time effect.**

***Keywords*—Switching flow-graph, virtual switch, virtual switching function, cascaded multilevel inverters.**

1. INTRODUCTION

The multilevel inverters are broadly used in power electrical systems recently due to the advantages of minimizing the total harmonic distortion (THD), producing more levels in the output voltages, and reducing the electromagnetic interference (EMI) emission. However, because of the nonlinear operation of switching components and the coupling between phase and phase, the modeling work of a multilevel inverter is very difficult. Therefore, the concept of virtual switch and virtual switching function are proposed to develop a graphic modeling tool, namely switching flow-graph (SFG) modeling technique, for cascaded full-bridge multilevel inverters in this research. The SFG modeling technique is first proposed in [1]-[3] to derive the model of DC-DC converters. Although, the SFG modelling technique is very easy to be used, the same technique is hard to be applied to model a circuit with different voltage polarity, like inverters or rectifiers [4].

In reference [5]-[7], the concept of virtual switch and virtual switching function is introduced to overcome the bottleneck of applying the SFG technique for modeling signal-phase and three-phase converters. By defining the virtual switch and virtual switching function, the trouble of using SFG technique to model the inverters or rectifiers are overcome. Moreover, the modeling process becomes very easy and without complicated mathematic operation.

This paper is organized as follows: In section 2, the concept of virtual switch and virtual switching function are introduced. Some simulation results are shown in section 3. Conclusions are given in section 4.

2. THE SFG MODELING TECHNIQUE FOR CASCADED MULTILEVEL INVERTERS

2.1. Review of SFG Modeling Technique

The modeling process of SFG technique can be introduced as follows [7]:

1) Find out all the qualified switching states according to the all possible switching operations.
2) Define the virtual switches and virtual switching functions based on the qualified switching states.
3) Plot the equivalent circuit with the virtual switches.

4) According to the switching operation of each virtual switch to draw the corresponding flow-graphs for all the sub-circuits with the same node distribution. [2]
5) Combine the flow-graphs with switching branches to obtain the switching flow-graph.
6) Change the switching branches by their large-signal switching branch model to obtain the corresponding large-signal SFG model.

A typical single-phase PWM inverter, as shown in Fig. 1, is used as an example. The S_{jP}, S_{jN} and D_{jP}, D_{jN}, $j \in \{A, B\}$ represent the controllable switches and uncontrollable diodes, respectively and the circuit is connected with a RL impedance load. Consider the switches and diodes of j-phase, there are sixteen possible switching-states for 4 switching devices. However, only six switching states are qualified under the assumption of (i) the switches of the same-phase will not be turned ON at the same time and (ii) the switches of the same-phase will not be operated in an open-state.

TABLE 1 QUALIFIED SWITCHING STATES FOR j-PHASE

Value of V_{jN}	*State Number*	*Switching States* $(S_{jP}, D_{jP}, S_{jN}, D_{jN})$
$V_{jN} = V_D$	*State 1*	*(OFF, ON, OFF, OFF)*
	State 2	*(ON, OFF, OFF, OFF)*
	State 3	*(ON, ON, OFF, OFF)*
$V_{jN} = 0$	*State 4*	*(OFF, OFF, OFF, ON)*
	State 5	*(OFF, OFF, ON, OFF)*
	State 6	*(OFF, OFF, ON, ON)*

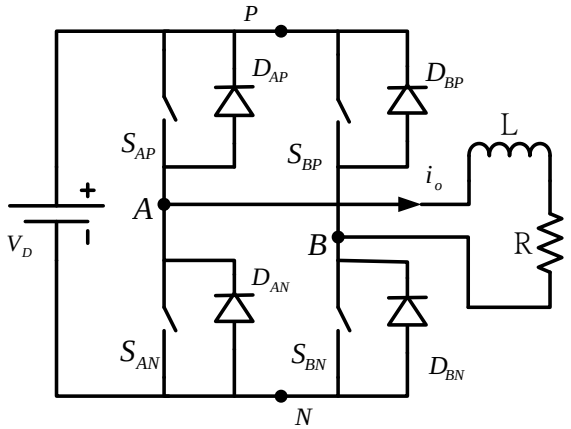


Fig. 1 The circuit of the single-phase inverter.

As shown in TABLE 1, one can see that the condition of $i_j < 0$ are occurred in state 2, 4 and 6; and the condition of $i_j > 0$ are occurred in state 1, 3 and 5. Form reference [2], the switching functions can be defined as equations (1) and (2).

$$F_{S_{jk}}(t) = \begin{cases} 1, & \text{when } S_{jk} \text{ is ON} \\ 0, & \text{when } S_{jk} \text{ is OFF} \end{cases} \quad (1)$$

$$\overline{F_{S_{jk}}}(t) = \begin{cases} 1, & \text{when } S_{jk} \text{ is OFF} \\ 0, & \text{when } S_{jk} \text{ is ON} \end{cases} \quad (2)$$

$$j \in \{A, B\},\ k \in \{P, N\}$$

According to the qualified switching states, one can defined the switching functions of D_{jk} as following:

If $\left[\left(S_{jN} \text{ is OFF}\right) \text{AND} \left(i_j(t) > 0\right)\right]$ is true
then D_{jP} is ON; otherwise, D_{jP} is OFF.

If $\left[\left(S_{jP} \text{ is OFF}\right) \text{AND} \left(i_j(t) < 0\right)\right]$ is true
then D_{jN} is ON; otherwise, D_{jN} is OFF.
$j \in \{A, B\}$

The switching functions of the diodes can be further defined as equations (3) and (4).

$$F_{D_{jP}}(t) \overset{\Delta}{=} \begin{cases} 1, & \text{when } D_{jP} \text{ is ON} \\ 0, & \text{when } D_{jP} \text{ is OFF} \end{cases} = \overline{F_{S_{jN}}(t)} \,\text{AND}\, \left(sign(-i_j)\right) \quad (3)$$

$$F_{D_{jN}}(t) \overset{\Delta}{=} \begin{cases} 1, & \text{when } D_{jN} \text{ is ON} \\ 0, & \text{when } D_{jN} \text{ is OFF} \end{cases} = \overline{F_{S_{jP}}(t)} \,\text{AND}\, \left(sign(i_j)\right) \quad (4)$$

$$sign(x) \overset{\Delta}{=} \begin{cases} 1\ , & x > 0 \\ 0\ , & x < 0 \end{cases} \quad (5)$$

$$j \in \{A, B\}$$

From TABLE 1, the virtual switch S_j can be defined as:

If $\left\{\left[\left(S_{jP} \text{ is ON}\right) \text{AND} \left(i_j > 0\right)\right] \text{OR} \left(D_{jP} \text{ is ON}\right)\right\}$ is ture
then S_j is ON; otherwise, S_j is OFF.
$j \in \{A, B\}$

The corresponding virtual switching function of S_j can be defined as:

$$F_j(t) \triangleq \begin{cases} 1, \text{when } S_j \text{ is ON} \\ 0, \text{when } S_j \text{ is OFF} \end{cases}$$

$$= \left[F_{S_{jP}}(t) \text{ AND } \left(sign\left(i_j\right)\right)\right] \text{OR } \left(F_{D_{jP}}(t)\right) \quad (6)$$

$$\overline{F_j}(t) \triangleq \begin{cases} 1, \text{when } S_j \text{ is OFF} \\ 0, \text{when } S_j \text{ is ON} \end{cases}$$

$$= \left[F_{S_{jN}}(t) \text{ AND } \left(sign\left(-i_j\right)\right)\right] \text{OR } \left(F_{D_{jN}}(t)\right) \quad (7)$$

$$F_j(t) + \overline{F_j}(t) = 1 \quad (8)$$
$$j \in \{A,\ B\}$$

From the definition of the virtual switches and the virtual switching functions, one can easily obtain the equivalent circuit of single-phase inverter with 2 virtual switches as plotted in Fig. 2.

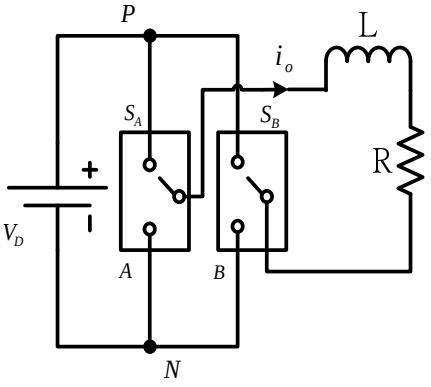


Fig. 2 Equivalent circuit of Fig. 1.

One can also present the virtual switches in graphic form by using AND-gate and OR-gate as described in Fig. 3.

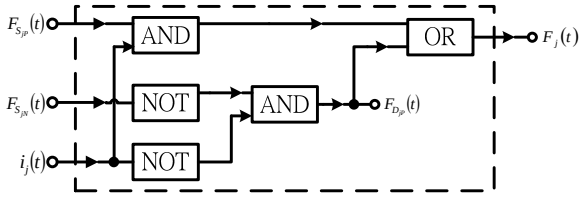


Fig. 3 The corresponding virtual switching function for j-phase.

2.2. The SFG Large-Signal Model for Cascaded Multilevel Inverters

By following the modeling procedures described in [7], the SFG large-signal model of cascaded multilevel inverters can be developed easily. Fig. 4 demonstrates the circuit of a 5-level cascaded inverter that is used as an example in this paper. There are eight controllable switches and eight uncontrollable diodes in the circuit. One can replace each phase of the circuit with one virtual switch based on the concept of the virtual switching function. Therefore, Fig. 4 can be modified to be an equivalent circuit as shown in Fig. 5.

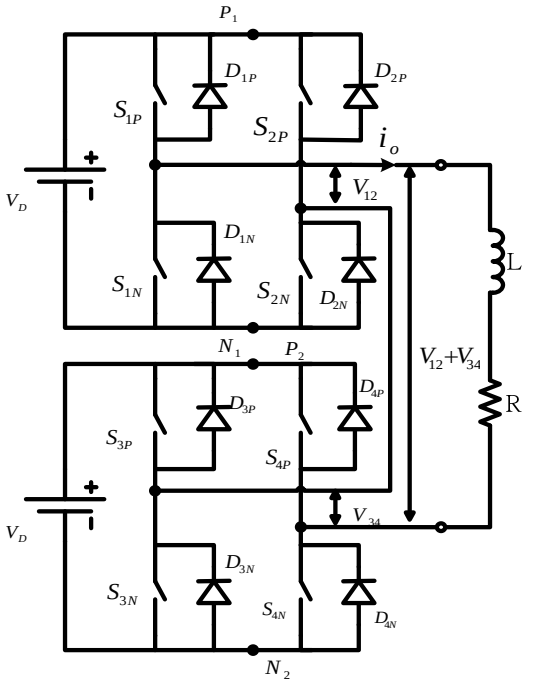


Fig. 4 The circuit of a 5-level cascaded inverter.

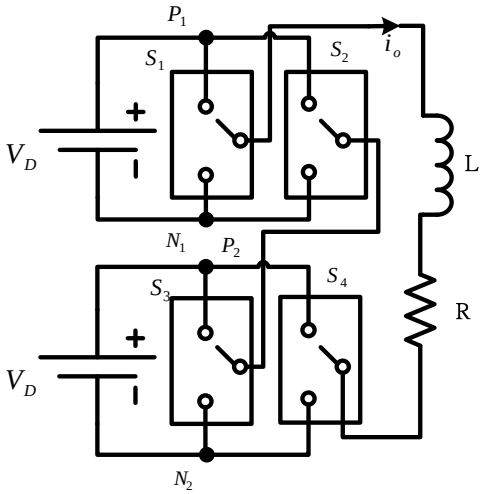


Fig. 5 The equivalent circuit of Fig. 4 with virtual switches.

According to Fig. 5, one can follow the modeling procedure of SFG to create the SFG large-signal model as plotted in Fig. 6. From Fig. 6, one can observe that the SFG model is very similar to the simulation structure in MATLAB/SIMULINK environment. Hence, it is very easy to implement the SFG large-signal model in MATLAB/SIMULINK environment to get the simulation results without requiring other extra efforts.

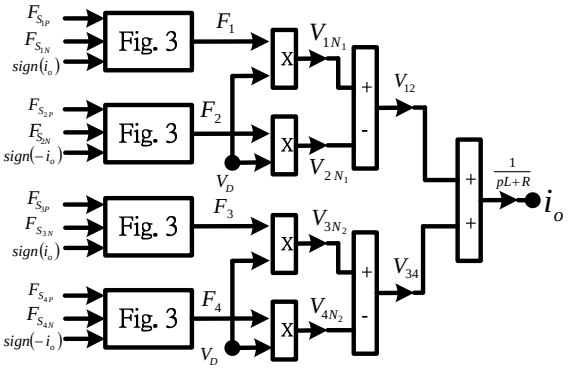


Fig. 6 The SFG large-signal model of a 5-level cascaded inverter.

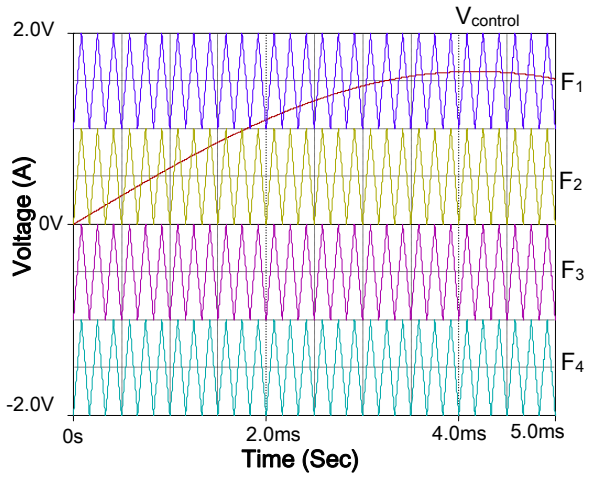


Fig. 7 PD-PWM schemes for 5-level cascaded inverter.

3. SIMULATION RESULT

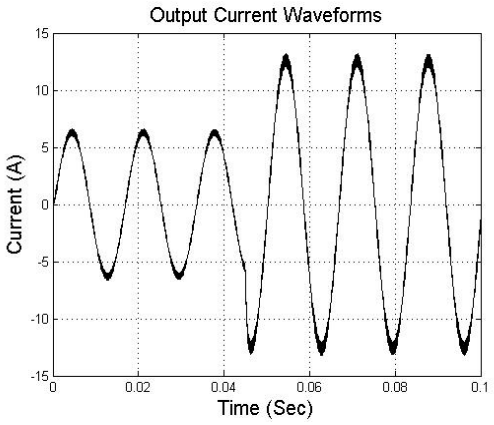
Fig. 4 is used as an example in this section, where the connected impedance load is set to be R=63 Ω and L=17.75 *mH* and the switching frequency f_s is equal to 6*k Hz*. Fig. 7 shows the PD-PWM waveforms used for the switches control in this simulation. The voltage command is set as follows:

$$V^*_{control}(t) = 1.6\sin(120\pi t)$$

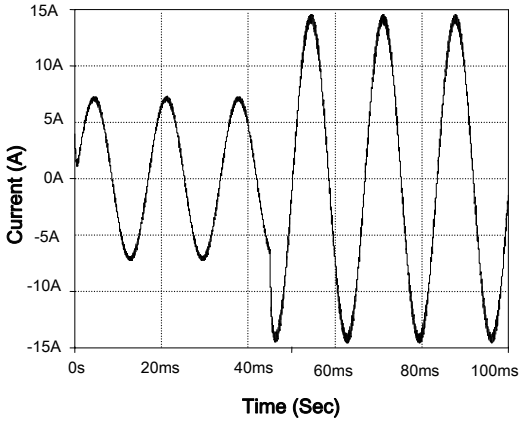
Example 1：

When blanking-time is equal to zero:

Fig. 8 shows the waveforms of output current. Fig. 8(a) and 8(b) are generated by using SFG model and PSPICE model respectively. One can see that the simulation results of the propose SFG model are well confirmed with the results generated from PSPICE. When the simulation time is set to be 200-ms, the execution time of using SFG model is 37.4 secs. However, the execution time of using PSPICE model is 88.22 secs under the same simulation condition.



(a)



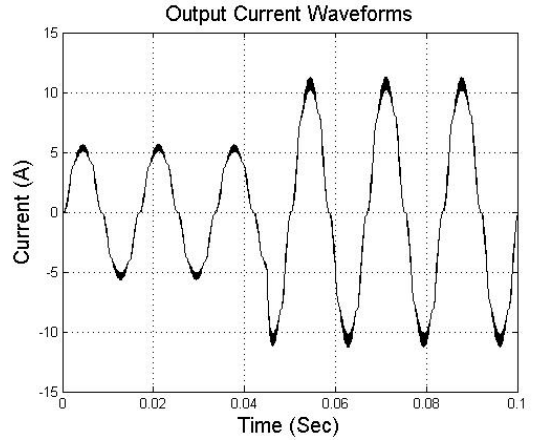
(b)

Fig. 8 The simulation results of the output current by using (a) the proposed SFG model, and (b) PSPICE model.

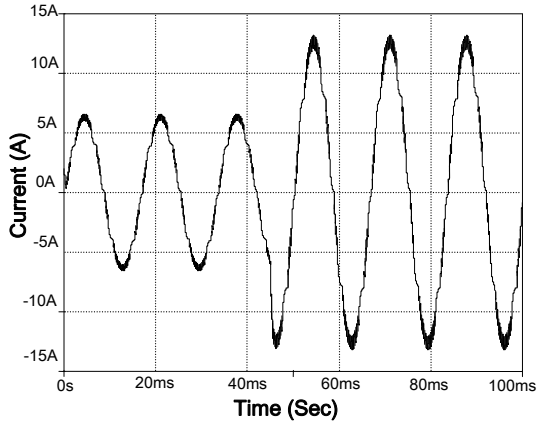
Example 2：

When blanking-time is equal to $40\mu s$:

The waveforms of the output current are shown in Fig. 9. The load is changed to be half of the original value at 0.045 sec. When the simulation time is set to be 200-ms, the execution time of using SFG model is 22.2 secs. However, the execution time of using PSPICE model is 146.23 secs under the same simulation condition.



(a)



(b)

Fig. 9 The simulation results of the output current by using (a) the proposed SFG model, and (b) PSPICE model.

The simulation is executed on a PC with Intel Core2 2.0GHz CPU / 1 GB RAM and the maximum step size of time-domain simulation is $2\mu s$. However, the computation time required by using the proposed switching flow-graph model is much less than that required by using PSPICE. Both simulation results agree with each other rather closely, which reveals that the switching flow-graph model can correctly predict the dynamic response, such as the start-up and load variation transients.

4. CONCLUSIONS

A SFG large-signal model of 5-level cascaded inverters is developed in this paper. By using the concept of virtual switch and virtual switching function, the modeling work of the cascaded multilevel inverter becomes easy and without complex mathematics operations. The simulation results show that by using the SFG model, one can obtain the desired waveforms that is closely confirmed with the simulated waveforms generated from PSPICE model. However, under the same simulation condition with nonzero blanking time, the SFG model requires only 1/6 execution time of using PSPICE model.

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